OBLON
SPIVAK
McCLELLAND
MAIER
&
NEUSTADT
P.C.

ATTORNEYS AT LAW

Docket No.: 0057-2534-2YY DIV

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

RE: Application Serial No.: 09/429,283
Applicants: Shuichi UENO, et al.
Filing Date: October 28, 1999
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME
Group Art Unit: 2823
Examiner: George R. Fourson, III

SIR:

Attached hereto for filing are the following papers:

APPEAL BRIEF (in triplicate)

Our check in the amount of $320.00 is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Attorney of Record
Registration No. 25,599
W. Todd Baker
Registration No. 45,265

Robert C. Mattson
Registration No. 42,850

22850

(703) 413-3000 (phone)
(703) 413-2220 (fax)
I:\atty\Wtb\0057\00572534\Sht PTO ltr.wpd

#18 Appeal Brief Acted 5/24/02

0057-2534-2YY DIV

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

Shuichi UENO et al. : GROUP ART UNIT: 2823

SERIAL NO: 09/429,283 :

FILED: October 28, 1999 : EXAMINER: G. FOURSON, III

FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

APPEAL BRIEF

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

This is an appeal of the Final Rejection dated December 18, 2001, of Claims 14-27 hereinafter referred to as the FR. A Notice of Appeal was timely filed on March 18, 2002.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is MITSUBISHI DENKI KABUSHIKI KAISHA having a place of business at 2-3, Marunouchi 2-chome ,Chiyoda-ku, Tokyo 100 Japan.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative, and the assignees are aware of no appeal which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 14-27 stand finally rejected, which final rejection forms the basis for this appeal. A copy of Claims 14-27 appears in the attached Appendix.

IV. STATUS OF THE AMENDMENTS

No amendments have been filed after the FR.

V. SUMMARY OF THE INVENTION

The present invention is directed to a novel method for manufacturing a semiconductor device having at least two types of transistors formed on a single substrate. The method is disclosed on page 114 line 13 - page 123 line 23 of the specification. Figures 63 - 70 of the specification correspond with that disclosure. The novel method includes the steps of forming first and second regions where first and second transistors are to be formed; forming a control electrode (or control electrodes); and selectively introducing nitrogen and/or impurities into the control electrode(s).

VI. ISSUES

The issue on appeal is whether or not the subject matter of claims 14-27 are unpatentable "over the combination of Japanese Patent 4-157766, Gardner et al. '849, Choi '330, Chou et al (1977 IEEE), Kurol et al. (J. Appl. Phys. 1995) and Sze ...."

VII. GROUPING OF THE CLAIMS

Claim 15 stands or falls with representative Claim 14.

Claims 17 and 18 stand or fall with representative claim 16.

Claims 20-27 stand or fall with representative claim 19.

VIII. ARGUMENT

A. REPRESENTATIVE CLAIM 14

1. Introduction

For the convenience of the Board, representative claim 14 is provided below:

14. A method of manufacturing a semiconductor device in which there are first and second types of transistors formed on a single semiconductor substrate, comprising the steps of:

(a) selectively forming a field oxide film on a main surface of said semiconductor substrate to thereby define first and second regions in which said first and said second types of transistors are formed;

(b) forming an oxide film on said first and said second active regions; and

(c) forming a control electrode of a polysilicon layer on said first and said second regions,

wherein said step (c) includes the steps of:

(c-1) introducing an impurity of the same conductivity as a source/drain layer into said polysilicon layer within said first region at a relatively low dose n1; and

(c-2) introducing said impurity into said polysilicon layer within said second region at a relatively high dose n2 while introducing nitrogen into a lower portion of said polysilicon layer within said second region at a dose n3.

2. The Ground for the Final Rejection of Claim 14

The thrust of the rejection of claim 14 is that each of a plurality of patents/publications teach or suggest a feature defined by claim 14 and that it would have

been obvious to combine those teachings in order to obtain the invention defined by claim 14.

3. *Prima Facie* Case Requirements

a. Graham Analysis

The FR completed only one of the three inquiries required by Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966). That is, the FR determined the scope and contents of the prior art.[1] The FR, however, failed to identify a primary reference on which the obviousness conclusion is based or to make a finding of the differences between the subject matter of claim 14 and that primary reference (or any reference). See Graham, 383 U.S. at 17-18 and 148 USPQ at 467. Because no differences were expressly identified, it follows that the FR also failed to determine whether the invention of claim 14 as a whole would have been obvious in view of those differences. Consequently, in view of the FR's deficient Graham inquiry, a *prima facie* case of obviousness was not made with regard to claim 14.

b. The Prior Art References When Combined must Teach or Suggest All the Claim Limitations

Moreover, in order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, other basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The cited prior art references, alone or in combination, do not teach or suggest all of the features of claim 14. This is evident and apparent, as none of the cited prior art references disclose, teach, or suggest the step of introducing an impurity into a polysilicon layer within a first region and a second region, wherein the impurity in the first region is at a relatively low dose and the impurity in the second region is at a relatively high dose.

---

[1]This appeal brief refers to the applied patents and publications as "prior art" for the sake of simplicity. However, Appellants note that the Gardner et al. and Choi references can be removed as prior art by perfecting priority.

Japanese Patent Publication No. 04157766 relates to the manufacture of a silicon gate p-channel MOSFET. This reference discloses a selective oxide film 3 and a gate oxide film 4 formed on substrate 1. A polyside film 7 made of p-type polysilicon film 5 and a tungsten silicide film 6 is formed. An n-channel MOSFET is masked with resist film 8. Nitrogen ions are then implanted into the p-channel MOSFET. Unlike the requirement of claim 14, Japanese Patent Publication No. 04157766 does not disclose introducing an impurity into a polysilicon layer within a first region at a relatively low dose and within a second active region at a relatively high dose. Accordingly, this reference is deficient in teaching or suggesting all the limitations defined by claim 14.

Choi relates to a selective diffusion process for forming both n-type and p-type gates with a single masking step. The June 14, 2001 office action cites Figures 3A - 3C and the specification in column 8, line 16-18. Figures 3A - 3C illustrate the formation of p-channel devices with p-type and n-type polysilicon gates and n-channel devices with n-type and p-type polysilicon gates. The disclosed polysilicon layer 200 is rendered to be p-type conductive by a blanket implant or by diffusion. It is further disclosed that the polysilicon layer 200 is divided into four portions (200a-200d). It is disclosed that portions 200a and 200b are counter-doped to be n-type conductive. However, the Choi disclosure does not alleviate the above-mentioned deficiencies of Japanese Patent Publication No. 04157766. This is evident and apparent, as the disclosure of Choi does not teach or suggest introducing an impurity in first and second active regions, wherein impurity is a relatively low dose within the first region and a relatively high dose within the second region. There is no disclosure in Figures 3A-3C or the accompanying description in column 5 of an impurity with different concentrations in the respective first and second active regions. As portions 200a and 200b

are disclosed as being counter-doped, these portions inherently do not have the same impurity as portions 200c and 200d in a different concentration.

Gardner et al. relates to a method of making an asymmetrical IGFET with a silicide contact on the drain without a silicide contact on the source. The June 14, 2001 office action cites column 10, lines 19-26 and column 12, lines 1-11. The June 14, 2001 office action asserts that "Gardner et al. discloses the dependence of threshold voltage on concentration of dopant in the gate of a MOSFET and the formation of MOSFET's having different concentrations of dopant on the same wafer..." Applicants traversed that assertion, as Gardner et al. merely discloses a single n-channel device. Gardner et al. discloses in column 10, lines 16-26 that a photoresist layer is provided over an IGFET that can cover substantially all of the gate, substantially none of the gate, or various amounts in between. It is disclosed that the photoresist layer can be used to adjust the threshold voltage of the gate. However, this disclosure does not accommodate for the introduction of impurity in a first active region at a relatively low dose and then a second active region at a relatively high dose. This is apparent because in contrast to claim 14, Gardner et al. is directed merely to formation of a single transistor in a single active region. Accordingly, Gardner et al. does not alleviate the deficiencies of Japanese Patent Publication No. 04157766 or Choi.

Chou et al. does not disclose a step of introducing an impurity within a first active region in a relatively low dose and introducing the impurity into a second region at a relatively high dose as defined by claim 14. Accordingly, Choi et al. does not alleviate the above-mentioned deficiencies of Japanese Publication Patent No. 04157766, Choi, or Gardner et al.

Kuroi et al. relates to the impact of nitrogen implantation into a highly doped polysilicon gate. The June 14, 2001 office action states that Kuroi et al. discloses the effects

of different nitrogen concentrations and dope concentrations in the gate of a MOSFET and cites Figures 2 and 3. However, Figures 2 and 3 and the accompanying disclosure on page 772 does not disclose or suggest the impact of relative dopant concentrations in the gates of adjacent transistors. Moreover, the Kuroi et al. disclosure does not teach or suggest introducing an impurity into the polysilicon layer within a first region and a second region, wherein the impurity in the first region is at a relatively low dose and the impurity in the second region is at a relatively high dose. Accordingly, the disclosure of Kuroi et al. does not alleviate the above-mentioned deficiencies of either Japanese Patent Publication No. 04157766, Choi, Gardner et al., or Chou et al.

Consequently, the applied patents and publications when combined do not teach or suggest all of the claim limitations defined by claim 14.

c. Motivation to Combine Should be Provided

There must also be some suggestion or motivation in the references themselves to modify the reference or to combine reference teachings. Hence, although Japanese Patent Publication No. 04157766 teaches selective implantation of Nitrogen into the polysilicon layer 200 of a first transistor. The FR fails to provide any motivation for why a person of ordinary skill in the art would modify the manufacture of the device described in the abstract of Japanese Patent Publication No. 04157766 to include the step of introducing an impurity into the polysilicon layer within a first region and a second region, wherein the impurity in the first region is at a relatively low dose and the impurity in the second region is at a relatively high dose. Appellants respectfully submit that the FR's reliance on Chou and Kuroi for motivation amounts to little more than hand waving. That is, although both Chou and Kuroi are related to the effects of implanting nitrogen and Kuroi is related to implanting nitrogen into highly doped gates, neither of those publications discloses the step of introducing

relatively low and high amounts of impurities into the polysilicon layers of a first and a second region, respectively, wherein the second region has been implanted with nitrogen or suggests the impact of doing so. Consequently, Applicants respectfully submit that the FR provides no motivation for combining the applied patents and publications.

Finally, there must be particular finding as to the specific understanding or principle within the knowledge of a skilled artisan that would have motivated one with no knowledge to the claimed invention to combine or modify references. *In re Kotzab*, 217 F.3d 1365, 55 U.S.P.Q.2d 1313 (Fed. Cir. 2000). Also, see M.P.E.P. §2143. The FR fails to make such a finding.

B. REPRESENTATIVE CLAIM 16

1. Introduction

For the convenience of the Board, representative claim 16 is provided below:

16. A method of manufacturing a semiconductor device in which there are at least two types of transistors on a semiconductor substrate, comprising the steps of:

(a) forming said first type of transistor in a first region of said device;

(b) forming said second type of transistor in a second region of said device; and

(c) forming a control electrode, which includes an impurity and nitrogen, in each of said first and second transistors;

(d) masking said first type of transistor, and

(e) introducing nitrogen into said control electrode of only said second type of transistor.

2. The Ground for the Final Rejection of Claim 16

The thrust of the rejection of claim 16 is the same as that of claim 14. That is, the FR and the June 14, 2001 office action do not distinguish between the independent claims although those claims define features which are not common to all of the independent claims.

3. *Prima Facie* Case Requirements

a. Graham Analysis

Just as the Graham analysis was not completed with regard to claim 14, the FR completed only one of the three inquiries required by Graham with regard to claim 16. That is, the FR determined the scope and contents of the prior art. The FR, however, failed to identify a primary reference on which the obviousness conclusion is based or to make a finding of the differences between the subject matter of claim 16 and that primary reference (or any reference). See Graham, 383 U.S. at 17-18 and 148 USPQ at 467. Because no differences were expressly identified, it follows that the FR also failed to determine whether the invention of claim 16 as a whole would have been obvious in view of those differences. Consequently, in view of the deficient Graham inquiry, a *prima facie* case of obviousness was not made in the FR with regard to claim 16.

b. The Prior Art References When Combined must Teach or Suggest All the Claim Limitations

Moreover, in order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, other basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The cited prior art references, alone or in combination, do not teach or suggest all of the requirements of claim 16. Claim 16 defines a step of forming a control electrode, which includes an impurity and nitrogen, in

each of a first and second transistor. The method comprises a subsequent step of masking the first transistor. The method further comprises a subsequent step of introducing nitrogen into the control electrode of only the second transistor.

Japanese Patent Publication No. 04157766 does not anticipate all of the limitations of claim 16 as there is no disclosure of forming a control electrode which includes an impurity and nitrogen in each of the first and second transistors. Accordingly, Japanese Patent Publication No. 04157766 is deficient in teaching or suggesting all of the claimed limitations required by claim 16.

Gardner et al. does not alleviate the above-mentioned deficiencies of Japanese Patent Publication No. 04157766. This is evident and apparent, as Gardner et al. does not disclose a method comprising the steps of forming a control electrode, which includes an impurity and nitrogen, in each of the first and second transistors and masking a first transistor and a subsequent step of introducing nitrogen into the gate electrode of only a second transistor. Gardner et al merely relates to a single transistor.

Neither Choi, Chou et al., nor Kuroi et al. alleviate the above-mentioned deficiencies of Japanese Patent Publication No. 04157766 or Gardner et al. This is evident and apparent, as these references contain no disclosure of forming a control electrode, which include an impurity and nitrogen in each of a first and second transistor, wherein the first transistor is masked and nitrogen is introduced into the control electrode of only the second transistor.

Consequently, the applied patents and publications when combined do not teach or suggest all of the claim limitations defined by claim 16.

C. REPRESENTATIVE CLAIM 19

1. Introduction

For the convenience of the Board, representative claim 19 is provided below:

19. A method of manufacturing a semiconductor device having first and second transistors on a main surface of a semiconductor substrate of a first conductivity type, comprising the steps of:

(a) forming an isolation film on said main surface of said semiconductor substrate for isolating said first and said second transistors;

(b) forming a gate insulation film of said first and said second transistors on said main surface of said semiconductor substrate;

(c) forming first and second control electrodes on said gate insulation film of said first and said second transistors, said first control electrode including an impurity of a second conductivity type and nitrogen of a first concentration, and said second control electrode including nitrogen of a second concentration different from said first concentration; and

(d) forming first and second source/drain regions on said main surface of said semiconductor substrate, respectively, at regions where said first and said second transistors are formed.

2. The Ground for the Final Rejection of Claim 19

The thrust of the rejection of claim 19 is the same as that of claims 14 and 16. That is, the FR and the June 14, 2001 office action do not distinguish between the independent claims although those claims define features which are not common to all of the independent claims.

3. *Prima Facie* Case Requirements

a. Graham Analysis

Just as the Graham analysis was not completed with regard to claims 14 and 16, the FR completed only one of the three inquiries required by Graham with regard to claim 19. That is, the FR determined the scope and contents of the prior art. The FR, however, failed to identify a primary reference on which the obviousness conclusion is based or to make a finding of the differences between the subject matter of claim 19 and that primary reference (or any reference). See Graham, 383 U.S. at 17-18 and 148 USPQ at 467. Because no differences were expressly identified, it follows that the FR also failed to determine whether the invention of claim 19 as a whole would have been obvious in view of those differences. Consequently, in view of the deficient Graham inquiry, a *prima facie* case of obviousness was not made in the FR with regard to claim 19.

b. The Prior Art References When Combined must Teach or Suggest All the Claim Limitations

Moreover, in order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, other basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The cited prior art references, alone or in combination, do not teach or suggest all of the requirements of claim 19. Claim 19 defines a step of forming first and second control electrodes on a gate insulation film of a first and second transistors. The first control electrode includes an impurity of a second conductivity type and nitrogen of a first concentration. The second control electrode includes nitrogen of a second concentration different from the first concentration.

Japanese Patent Publication No. 04157766 does not teach or suggest all of the requirement of claim 19. This is an evident and apparent, as the disclosure does not teach or

suggest a first control electrode including nitrogen of a first concentration and a second control electrode including nitrogen of a second concentration. Neither Choi, Kuroi et al., Gardner et al. nor Chou et al. alleviate this deficiency of Japanese Patent Publication No. 04157766.

Consequently, the applied patents and publications when combined do not teach or suggest all of the claim limitations defined by claim 19.

CONCLUSION

The FR clearly fails to present a *prima facie* case as to obviousness. Therefore, reversal of all rejections is believed to be in order.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Registration No. 25,599
Attorney of Record
W. Todd Baker
Registration No. 45,265

22850

Robert C. Mattson
Registration No. 42,850

(703) 413-3000
Fax #: (703) 413-2220
GJM:WTB:jmr

I:\atty\Wtb\0057\00572534\Appeal Brief.wpd

APPENDIX

14. A method of manufacturing a semiconductor device in which there are first and second types of transistors formed on a single semiconductor substrate, comprising the steps of:

(a) selectively forming a field oxide film on a main surface of said semiconductor substrate to thereby define first and second regions in which said first and said second types of transistors are formed;

(b) forming an oxide film on said first and said second active regions; and

(c) forming a control electrode of a polysilicon layer on said first and said second regions,

wherein said step (c) includes the steps of:

(c-1) introducing an impurity of the same conductivity as a source/drain layer into said polysilicon layer within said first region at a relatively low dose n1; and

(c-2) introducing said impurity into said polysilicon layer within said second region at a relatively high dose n2 while introducing nitrogen into a lower portion of said polysilicon layer within said second region at a dose n3.

15. The method of manufacturing a semiconductor device of claim 14, wherein said dose n1 is $5 \times 10^{14}/cm^2$, said dose n2 is $5 \times 10^{15}/cm^2$, and said dose n3 is $1 \times 10^{15}/cm^2$.

16. A method of manufacturing a semiconductor device in which there are at least two types of transistors on a semiconductor substrate, comprising the steps of:

(a) forming said first type of transistor in a first region of said device;

(b) forming said second type of transistor in a second region of said device; and

(c) forming a control electrode, which includes an impurity and nitrogen, in each of said first and second transistors;

(d) masking said first type of transistor, and

(e) introducing nitrogen into said control electrode of only said second type of transistor.

17. The method of manufacturing a semiconductor device of claim 16, comprising:

(f) forming at least three types of transistors in respective first second and third regions of said device;

(g) forming a control electrode, which includes an impurity and nitrogen, in each of said first, second and third transistors;

in step (e), introducing nitrogen into control electrodes of only said second and third transistors;

(h) masking said first and second transistors; and

(i) introducing nitrogen into only said control electrode of said third transistor.

18. The method of manufacturing a semiconductor device of claim 17, comprising:

(j) implanting nitrogen of doses n1, n2, and n3 into said control electrodes of said first, second and third transistors, respectively, where $n1 < n2 < n3$.

19. A method of manufacturing a semiconductor device having first and second transistors on a main surface of a semiconductor substrate of a first conductivity type, comprising the steps of:

(a) forming an isolation film on said main surface of said semiconductor substrate for isolating said first and said second transistors;

(b) forming a gate insulation film of said first and said second transistors on said main surface of said semiconductor substrate;

(c) forming first and second control electrodes on said gate insulation film of said first and said second transistors, said first control electrode including an impurity of a second conductivity type and nitrogen of a first concentration, and said second control electrode including nitrogen of a second concentration different from said first concentration; and

(d) forming first and second source/drain regions on said main surface of said semiconductor substrate, respectively, at regions where said first and said second transistors are formed.

20. The method of manufacturing a semiconductor device according to claim 19, wherein

said step (b) includes a step of

(b-1) forming a first insulation film on said main surface of said semiconductor substrate, at regions where said first and said second transistors are formed,

said step (c) includes the steps of:

(c-1) forming a polysilicon layer including an impurity of the second conductivity type on a surface of said first insulation film; and

(c-2) patterning said polysilicon layer.

21. The method of manufacturing a semiconductor device according to claim 20, wherein

said step (c-1) comprises the steps of:

introducing nitrogen into said polysilicon layer, at regions where said first and said second transistors are formed; and

masking over a surface at a region where said first transistor is formed, and introducing nitrogen further into said polysilicon layer, at a region where said second transistor is formed.

22. The method of manufacturing a semiconductor device according to claim 21, further comprising the step of

forming a capacitor which is connected to one of said second source/drain regions, after said step (d).

23. The method of manufacturing a semiconductor device according to claim 19 further comprising a third transistor on said main surface of said semiconductor substrate, wherein

said step (a) comprises a step of

forming said isolation film so as to isolate said first to third transistors,

said method, after said step (a) and before the step of forming said first insulation film, further comprising the steps of:

forming a second insulation film at a region where said third transistor is formed;

forming a conductive layer on a surface of said second insulation film;

and

forming a third insulation film on a surface of said conductive layer,

wherein

said step (c-1) includes the steps of:

forming said polysilicon layer also on a surface of said third insulation film, said polysilicon layer serving as a third control electrode and including an impurity of said second conductivity type;

introducing nitrogen into said polysilicon layer, at regions where said first to third transistors are formed, and

masking over a surface at a region where said first and third transistors are formed, and introducing nitrogen further into said polysilicon layer, at a region where said second transistor is formed, and

said step (c-2) comprises a step of

patterning said third insulation film, said conductive layer and said polysilicon layer.

24. The method of manufacturing a semiconductor device according to claim 19 wherein

said step (b) includes a step of

(b-1) forming a first insulation film on said main surface of said semiconductor substrate, at regions where said first and said second transistors are formed,

said step (c) includes the steps of:

(c-1) forming a polysilicon layer which does not include an impurity on a surface of said first insulation film;

(c-2) introducing an impurity of said conductivity type into said polysilicon layer to thereby form a doped polysilicon layer; and

(c-3) patterning said doped polysilicon layer.

25. The method of manufacturing a semiconductor device according to claim 24 further comprising, prior to said step (c-3), the steps of:

introducing nitrogen into said doped polysilicon layer, at regions where said first and said second transistors are formed; and

masking over a surface at a region where said first transistor is formed, and introducing nitrogen further into said doped polysilicon layer, at a region where said second transistor is formed.

26. The method of manufacturing a semiconductor device according to claim 25, further comprising a step of

forming a capacitor which is connected to one of said second source/drain regions, after step (d).

27. The method of manufacturing a semiconductor device according to claim 24, further comprising a third transistor on said main surface of said semiconductor substrate, where

said step (a) comprises a step of

forming said insulation film to isolate said first to third transistors,

said method, after said step (a) and before the step of forming said first insulation film, further comprising the steps of:

forming a second insulation film at a region where said third transistor is formed;

forming a conductive layer on a surface of said second insulation film; and

forming a third insulation layer on said main surface of said semiconductor substrate, wherein

said step (c-1) includes the steps of:

forming said polysilicon layer serving as a third control electrode also on a surface of said third insulation film,

said step (c-2) comprises a step of

introducing an impurity of said second conductivity type into regions where said first to third transistors are formed;

said method further comprises, prior to said step (c-3), the steps of:

introducing nitrogen into said doped polysilicon layer, at the regions where said first to third transistors are formed; and

masking over a surface at a region where said first and said third transistors are formed, and introducing nitrogen further into said polysilicon layer, at a region where said second transistor is formed, and

said step (c-3) comprises a step of

patterning said third insulation film, said conductive layer and said doped polysilicon layer.